

REMARKS/ARGUMENTS

Claim Amendments

The Applicant has amended claim 1. Applicant respectfully submits no new matter has been added. Accordingly, claims 1-16 and 18-24 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

Examiner Objections – Drawings

The Drawings were objected to in Figures 1-17 because the shading makes the labels in the drawings difficult to read. Corrections to the drawings are shown on the enclosed replacement sheets. The Examiner's approval of the drawing changes is respectfully requested.

Claim Rejections – 35 U.S.C. § 112

Claim 1 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter as the invention. The Applicant has corrected the deficiencies in claim 1 and the Applicant respectfully submit that claim 1 is now allowable.

Claim Rejections – 35 U.S.C. § 103 (a)

Claims 1-8, 10, 12-16, 19, 20 and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent Number (US 5,790,817) (Asghar) in view of US Patent Number (US 6,345,188) (Keskitalo et al). The Applicant respectfully traverses the rejection of these claims.

The Applicant respectfully directs the Examiner's attention to an excerpted limitation from claim 1:

1.

...at least one analog signal manifold comprising
input lines, output lines, and nodes for making connections
between input and output lines, said input lines and output lines being
connectable to predetermined resources and said nodes being arranged

to perform a mathematic operation on an incoming signal on the input lines.

The Applicant respectfully submits that a problem solved by the present invention is to provide low cost, flexible, signal processing in a radio base station. The analog signal manifold recited above is also defined in the Applicant's specification as a resource. "A specific resource is the manifold 39 (k). In one embodiment, one HF (High Frequency) manifold is foreseen combining all possible routings between HF components like DACs 41 (m), TXs 35 (i), ADCs 43 (n), RXs 37 (j) and signal generators (not shown; e. g. , necessary to generate signals with an intermediate frequency in GSM systems as is known to persons skilled in the art). The manifold 39 (k) includes simple operations like adding, subtracting or multiplication of analogue signals, as will be explained below." (page 6, line 31-page 7, line 4) The Applicant respectfully submits that the prior art cited does not disclose at least this limitation present in the independent claims of the present application

The Ashgar reference is cited for, among other things, disclosing an analog signal manifold as claimed in the limitation cited above. The portion of Ashgar that is cited discloses a "...[d]igital system includes analog to digital conversion logic ...and digital to analog conversion logic..." (col 8, lines 41-42). The Applicant respectfully submits that Ashgar, either in the cited portion or in the rest of the Ashgar reference, does not disclose an analog signal manifold, merely ADC and DAC conversion logic. As claimed, and disclosed in the Applicant's specification, the analog manifold does not convert the signals, but performs simple mathematical operations on incoming signals. In fact, the Applicant discloses in one embodiment, that of a Radio Base Station, a HF manifold that combines all routings between DACs, TXs, ADCs, RXs, and signal generators (Figure 9, page 26, lines 21-38). The manifold connects to DACs and ADCs, the manifold is not part of the DACs and ADCs. Further, the manifold is much like a high frequency matrix with analog functions like adding, subtracting or multiplying HF signals in the cross points of the matrix. Therefore, Ashgar does not disclose the above discussed limitations of claim 1 and the analogous claims

The Ashgar reference is noted as not disclosing an analog signal manifold comprising input lines and output lines and nodes for connecting between the input and output lines for performing a mathematical operation on incoming signals. The Keskitalo reference is cited for teaching an apparatus and method of steering a signal from a base station whereby at least one RX matrix performs phasing on an analog signal received by antenna elements so that output signals correspond to a signal received by an antenna beam pointing in a predetermined direction. A Butler matrix is also disclosed that uses passive hybrids and phase shifters to combine outputs to provide simultaneous signals. The Applicant does not disagree with the analysis of the Keskitalo reference. However, the Applicant does not believe that the principles of Keskitalo apply to the present invention.

Keskitalo discloses a basic phased array principle, used in, e.g., radio direction finders and military phased array radar. The basic principle is to delay analog signals that are fed to antenna elements. Essentially, Keskitalo merely applies a variable delay line that produces a phase shift of signals with the variable delay. Variable delay means that the input for a matrix point contains a data value representing the delay or this value is hard coded in the matrix. Also, delay is not a mathematical operation like the Applicant's invention which claims adding subtracting, etc. of analog signals.

Comparing the Applicant's matrix with the Keskitalo matrix: Keskitalo offloads on to DSP's by using a TX matrix with dedicated hardware, i.e., mathematical operations are performed in the TX matrix, but these operations are digital operation and can be performed in the DSP's. One of the reasons the Applicant is using analog is to offload the mathematical operations from the DSP's because with the present invention, these operations can be done in analog in real time. Another important point is that the Applicant's invention combines analog signal routing and mathematical operations in one matrix, which allows combining of receiver and transmitter signal like direct retransmission.

As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness, ... the prior art reference (or references when combined) must teach or suggest all the claim limitations." In that regard, the Applicant respectfully submits that the Examiner's

two references still fail to teach or suggest each and every element of the presently pending independent claims.

Contrary to the rejection in paragraph 11 of the Detailed Action that all elements are disclosed in the Ashgar reference; all the elements in claim 1 and analogous claim 16, are not disclosed or taught in either Ashgar or Keskitalo or a combination of both. Dependent claims 2-8, and 10, 12-16, 19, 20 and 22-24 include the patentable subject matter of claim 1, and the Applicant respectfully requests the allowance of these claims.

Claims 9, 11 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent Number 5,790,817 (Asghar) in view of US Patent Number 6,976,021 (Ramakrishnan). The Applicant respectfully traverses the rejection of these claims.

The Ramakrishnan reference is cited for disclosing re-usable resources whereby a DRAM memory stores a hash table and active doubly linked lists that are managed via a resource allocation module. However, the Ramakrishnan reference fails to provide the missing analog signal manifold disclosed by the Applicant in claims 1 and 16. Claims 9, 11 and 21 depend from claims 1 and 16 respectively and contain the same novel subject matter. This being the case, the applicant respectfully requests the allowance of claims 9, 11 and 21.

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



By Sidney L. Weatherford
Registration No. 45,602

Date: October 9, 2009

Ericsson Inc.
6300 Legacy Drive, M/S EVR 1-C-11
Plano, Texas 75024

(972) 583-8656
sidney.weatherford@ericsson.com